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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,677	DEVINS ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8,10-15 and 17-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8,10-15 and 17-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3-6, 8, 10-15, and 17-30 have been presented for examination.

Response to Arguments

2. Applicant's arguments with respect to claims **1, 3-6, 8, 10-15, and 17-20** have been considered but are moot in view of the new ground(s) of rejection.

With respect to the Applicants arguments regarding claim 14, although the limitations of claim 14 were addressed in the rejection of claim 7, they are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. **Claim 8 is rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 8 recites a software method. It is unclear how a method, which is a set of steps, can also be a piece of software. Software does not comprise steps, but rather a sequence of code that when executed can perform a set of steps. Claim 1 is not rejected under 35 U.S.C. 101 as it does recite an actual device.

All claims dependent upon rejected base claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1, 8, and 15 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites a software system but includes an external memory mapped test device which is hardware. It is unclear how the system can be software if an element of the system is embodied as hardware.

Claim 8 recites a software method but includes an external memory mapped test device which is hardware. It is unclear how the method can be software if an element of the system is embodied as hardware.

Claim 8 recites a software method. It is unclear how a method, which is a set of steps, can also be a piece of software. Software does not comprise steps, but rather a set of code that when executed can perform a set of steps.

Claims 1, 8, and 15 recite "programmably connectable." It is unclear what is meant by programmably connectable. It is unclear if this is hardware or software connected to another piece of hardware or software. Please refer to the specification when responding to the rejection.

All claims dependent upon rejected base claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim(s) 1, 3-6, 8, 10-15, and 17-20 and 30 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by **Evans et al. "Apparatus and Method for Verifying a Multi-Component Electronic Design", U.S. Patent No. 6,279,146,** hereafter referred to as **Evans.**

Regarding Claim 1:

Evans discloses A software system for verifying an integrated circuit design said system comprising:

an external memory mapped test device having a switch programmably connectable to one or more I/O driver models and to a simulated I/O controller, said I/O driver models connected to corresponding simulated I/O cores by corresponding virtual buses; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

a virtual memory bus connecting said I/O controller and said switch; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

and wherein said I/O cores and said I/O controller are software descriptions of said integrated circuit design. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 2:

Evans discloses The system of claim 1, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models. **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

Regarding Claim 3:

Evans discloses The system of claim 1, wherein said external memory mapped test device further includes an address register. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 4:

Evans discloses The system of claim 1 wherein said integrated circuit design further includes an embedded processor. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 5:

Evans discloses The system of claim 2, wherein each said external memory mapped test device module further includes an address register. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 6:

Evans discloses The system of claim 2, wherein said integrated circuit design further includes an embedded processor. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 7:

Evans discloses The system of claim 1, wherein said external memory mapped test device and said switch are distributed among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models and further including an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 8:

Evans discloses A software method for verifying an integrated circuit design the method comprising:

providing an external memory mapped test device software module having a switch programmably connectable to one or more I/O driver models and to a simulated I/O controller, said I/O driver models connected to corresponding simulated I/O cores by corresponding virtual buses; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

providing a virtual memory bus connecting said I/O controller and said switch; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

programming connections of said external memory mapped test device and connections of a general purpose I/O core to said I/O models; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

wherein said I/O cores, said general purpose I/O core, and said I/O controller are software descriptions of said integrated circuit design; and **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

simulating said integrated circuit design by running a test case with said programmed connections. **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

Regarding Claim 9:

Evans discloses The method of claim 8, further including: distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 10:

Evans discloses The method of claim 8, further including: providing said external memory mapped test device with an address register and setting said switch and controlling said I/O driver models using address information programmed into said address register. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 11:

Evans discloses The method of claim 8, further including: providing an embedded processor in said integrated circuit design, said embedded processor running said test operating system. **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

Regarding Claim 12:

Evans discloses The method of claim 9, further including: providing each external memory mapped test device with an address register and setting each portion of said switch and controlling each I/O driver model using address information programmed into said address register. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 13:

Evans discloses The method of claim 9, further including: providing said integrated circuit design with an embedded processor running said test case on said embedded processor. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 14:

Evans discloses A method for verifying an integrated circuit design comprising:

providing an I/O controller connected to one or more I/O cores, said I/O cores part of said integrated circuit design. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

providing an external memory mapped test device having a switch for selectively connecting one or more of said I/O cores to corresponding I/O driver models; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

providing a bus for transferring signals between said I/O controller and said switch; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

providing a test operating system for controlling said switch; **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

simulating said integrated circuit design by running a test case on said test operating system; **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

and providing an additional external memory mapped test device module directly connected to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 15:

Evans discloses A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for verifying an integrated circuit design, said method steps comprising:

providing an external memory mapped test device software module having a switch programmably connectable to one or more I/O driver models and to a simulated I/O controller, said I/O driver models connected to corresponding simulated I/O cores by corresponding virtual buses; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

providing a virtual memory bus connecting said I/O controller and said switch; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

programming connections of said external memory mapped test device and connections of a general purpose I/O core to said I/O models; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

wherein said I/O cores, said general purpose I/O core, and said I/O controller are software descriptions of said integrated circuit design; **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

and simulating said integrated circuit design by running a test case with said programmed connections. **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

Regarding Claim 16:

Evans discloses The program storage device of claim 15, said method steps further including: distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 17:

Evans discloses The program storage device of claim 15, said method steps further including: providing said external memory mapped test device with an address register and setting said switch and controlling said I/O driver models using address information programmed into said address register. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 18:

Evans discloses The program storage device of claim 15, said method steps further including: providing an embedded processor in said integrated circuit design said embedded processor running said test operating system. **(Column 12, Line 18 – Line 43. Figures 2 and 5)**

Regarding Claim 19:

Evans discloses The program storage device of claim 16, said method steps further including: providing each external memory mapped test device with an address register and setting each portion of said switch and controlling each I/O driver model using address information programmed into said address register. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 20:

Evans discloses The program storage device of claim 16, said method steps further including: providing said integrated circuit design further with an embedded processor running said test case on said embedded processor. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Regarding Claim 30:

Evans discloses The method of claim 8, further including:

distributing said external memory mapped test device and said switch among a plurality of external memory mapped test device modules, each module containing a portion of said switch and connected to one of said I/O driver models; **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

connecting an additional external memory mapped test device module directly to one or more additional I/O driver models, each additional I/O driver model directly connected to an additional I/O core, each additional I/O core part of said integrated circuit design. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of

each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claim(s) 21-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Evans** in view of **Dutta et al. "Viper"**, hereafter referred to as **Dutta .**

Regarding Claim 21:

Evans discloses The system of claim 1, wherein said one or more I/O cores are independently selected from the group consisting of universal asynchronous receiver transmitter cores, serial cores, and general purpose I/O cores. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Evans does not explicitly disclose The system of claim 1, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores.

Dutta discloses The system of claim 1, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the 1394 I/O core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Regarding Claim 22:

Evans discloses The system of claim 1, wherein said integrated circuit design further includes an embedded processor core, a memory controller core. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Evans does not explicitly disclose The system of claim 1, wherein said integrated circuit design further includes a direct memory access core.

Dutta discloses The system of claim 1, wherein said integrated circuit design further includes a direct memory access core. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the DMA core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Regarding Claim 23:

Evans does not explicitly disclose The system of claim 22, further including a direct memory access core model of said a direct memory access core.

Dutta discloses The system of claim 22, further including a direct memory access core model of said a direct memory access core. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the DMA core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Regarding Claim 24:

Evans discloses The method of claim 8, wherein said one or more I/O cores are independently selected from the group consisting of universal asynchronous receiver transmitter cores, serial cores, and general purpose I/O cores. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Evans does not explicitly disclose The method of claim 8, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores.

Dutta discloses The method of claim 8, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the 1394 I/O core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Regarding Claim 25:

Evans discloses The method of claim 8, wherein said integrated circuit design includes an embedded processor core, a memory controller core. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Evans does not explicitly disclose The method of claim 8, wherein said integrated circuit design includes a direct memory access core.

Dutta discloses The method of claim 8, wherein said integrated circuit design includes a direct memory access core. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the DMA core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Regarding Claim 26:

Evans does not explicitly disclose The method of claim 26, wherein said integrated circuit design includes a direct memory access core model of said a direct memory access core.

Dutta discloses The method of claim 26, wherein said integrated circuit design includes a direct memory access core model of said a direct memory access core. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the DMA core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Regarding Claim 27:

Evans discloses The program storage device of claim 15, wherein said one or more I/O cores are independently selected from the group consisting of universal asynchronous receiver transmitter cores, serial cores, and general purpose I/O cores. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Evans does not explicitly disclose The method of claim 8, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores.

Dutta discloses The method of claim 8, wherein said one or more I/O cores are independently selected from the group consisting of 1394 I/O cores. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the 1394 I/O core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Regarding Claim 28:

Evans discloses The program storage device of claim 15, wherein said integrated circuit design includes an embedded processor core, a memory controller core. **(Column 10, Line 60 – Column 11 Line 26. Figures 2 and 5)**

Evans does not explicitly disclose The program storage device of claim 15, wherein said integrated circuit design includes a direct memory access core.

Dutta discloses The program storage device of claim 15, wherein said integrated circuit design includes a direct memory access core. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the DMA core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Regarding Claim 29:

Evans does not explicitly disclose The program storage device of claim 27, wherein said integrated circuit design includes a direct memory access core model of said a direct memory access core.

Dutta discloses The program storage device of claim 27, wherein said integrated circuit design includes a direct memory access core model of said a direct memory access core. **(Page 21, Paragraph 3)**

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the DMA core discussed in **Dutta** for the system of **Evans** in order to allow for proper verification of all popular input output formats. In any case, the types of cores refer to intended use.

Conclusion

7. All Claims are rejected.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

March 30, 2006

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